CM1-COMBO

CompactPCI® Intelligent Mezzanine Carrier Board
for PC•MIP Modules

User's Manual

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About this Manual

This manual describes the technical aspects of the CM1-COMBO, required for installation and system integration. It is intended for the experienced user only.

Edition History

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Text # 1851 cm1mle.wpd	2	2. Edition User Manual CM1-COMBO English	gn	Febr. 2001
	3	Added chapter “About this Manual” set header font size to 12pt.	gn	2. April 2001

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

i960 RP: ® Intel
CompactPCI : ® PICMG
PC•MIP: ® MEN Micro, SBS Technologies
Windows 98, Windows NT, Windows 2000: ® Microsoft

EKF does not claim this list to be complete.

Legal Exclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

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Introduction and Overview

Modularity is the reason for their success: different mezzanine modules can be combined on a single carrier board in order to achieve a functionality tailored exactly with the target application in mind. Because the customer can profit from both, individual configuration of the system and moderate cost, mezzanine concepts as M-Modules, PMC-Modules or Industry Packs are very popular for industrial grade computers. Another advantage is the high density packaging as a result, compared to solutions where functions are distributed over several full sized boards.

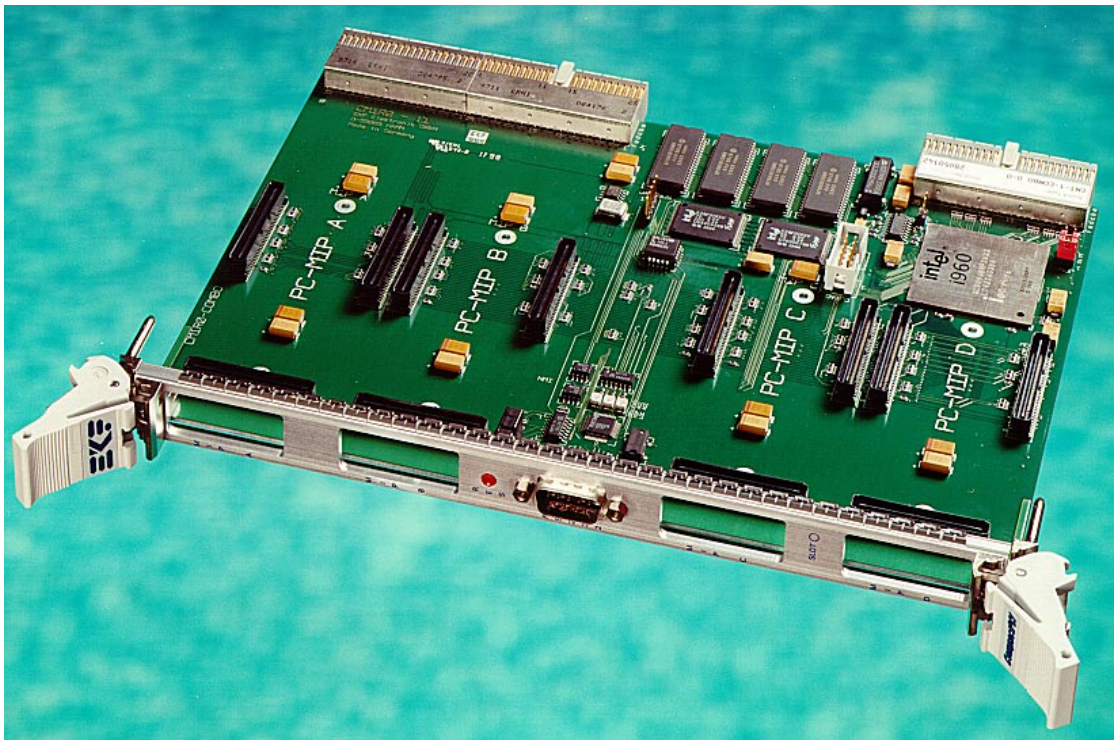
At the top of the evolution, the PC•MIP concept brings together the best characteristics of older mezzanine standards. EKF now unveils the CM1-COMBO, an i960® based, intelligent CompactPCI® carrier board for up to 4 PC•MIP modules.

The PC•MIP (PCI and M-Modules and Industry Packs) electrical characteristics are based on the well known PCI specification.

Regarding the mechanics, PC•MIP modules represent a smart and flexible successor to the M-Module technology.

The PC•MIP standard has been created by Motorola, GreenSpring and MEN; the specification is currently available as VITA draft (submitted as ANSI standard, to be released soon). There can be no doubt that PC•MIP will determine the trend in mezzanine modules for many years.

For best results, PC•MIP mezzanine modules should be used together with an intelligent carrier board as the CM1-COMBO. Need a real- time solution? Take that.



***CompactPCI*® PC•MIP Carrier Module CM1-COMBO**

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Based on the i960®RP embedded processor on-board, the CM1-COMBO is equipped with both, a powerful CPU, and a PCI bridge used as interface to the CompactPCI® system bus. 8 MB DRAM and 4 MB Flash EEPROM build a generous local memory resource for program and data. The on-board (16C550 based) serial communications interface can be connected to external peripherals, e.g. as a diagnostic port.

The CM1-COMBO can be populated with up to 4 PC•MIP modules of the type I (I/O wired across the rear CompactPCI® connectors J4/J5), or type II (with front panel mounted connectors). Neighboring PC•MIP slots can hold double size modules.

When developing self-written software for the CM1-COMBO, 3 on-board LEDs, representing i960- and board-status information, are a valuable help. Reset- and NMI- push button switches can be activated from the front panel.

The CM1-COMBO hardware supports the I_2O interface. This is a layered, standardized driver concept, modeled after the OSI reference, suitable especially for intelligent I/O sub-processors.

For any different class of I_2O devices, the hosts operating system has to be provided with an Operating System Service Module (OSM). This is a hardware abstract I_2O driver layer, just converting standardized I_2O commands to proprietary I/O system calls of the individual OS, e.g. Windows-NT (from version 5).

On the target device side (the CM1-COMBO) runs a Hardware Device Module (HDM). This driver interprets commands of the I_2O abstract OSM layer, with concrete I/O activities as the result. The HDM layer does not depend on any specific OS.

An I_2O communications layer between the OSM and HDM layers allows for flexible data exchange, not only between host-CPU and I/O subsystem, but also between the sub-processors without charging the host (with version 2.0 of the I_2O specification).

Use of the intelligent CM1-COMBO frees the host-CPU from critical low level tasks, an essential criterion for real-time applications. Because the COMBO can be equipped with a wide variety of PC•MIP modules, it is a smart and flexible solution to many different industrial applications, offering a fast time to market at moderate cost.

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EKF - Solutions Inside!

i960® Intel, CompactPCI® PICMG, PICMG ® PCI Industrial Computers Manufacturers Group

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Handling Information

Precautions

This *CompactPCI* ® board contains **electrostatic sensitive** devices. The board should therefore remain in its original EKF packaging until it is used. The antistatic coated film and box provide double protection against electromagnetic discharging as well as against dust, corrosion and mechanical damaging. Be sure to equalize the electrical potential of the board and the *CompactPCI* ® rack before taking out the board of the packaging (by touching the packaging and metallic parts of the rack at the same time, or better by wearing a ground strap). Please keep the original packaging for the case of return. Notice that installing or removing of boards or other system components may done only by authorized persons.

Guidelines to EMC Protection

To fulfill the **CE** specifications with regard to **EMC** take notice of the following guidelines:

- Installation and operation only in EMC systems.
- Close unused system slots with dummy panels.
- Close unused front elements (e.g. RS-232 interfaces) with metallic caps.
- Use shielded cables only.
- Use ferrites to prevent electromagnetic interference (EMI).
- Protect sensible interfaces (e.g. Cheapernet) with plastic caps.

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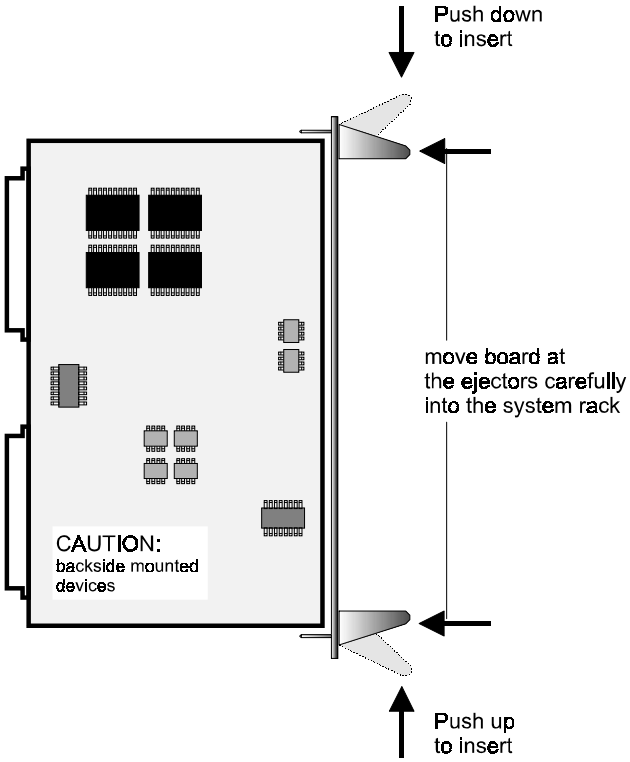
Installing boards

- Switch off the main power supply.
- Touch the system rack to guarantee electrostatic discharge.
- Move board carefully along the guide rails in the chosen slot of the rack. Caution is given especially to the devices mounted on the backside of the circuit board.
- Press the *CompactPCI* ® connectors of the board into the backplane receptacles by pushing the ejectors in the front panel together (see illustration below).
- Optionally screw board and rack together.
- Switch on the main power supply.



Installing board into the system rack

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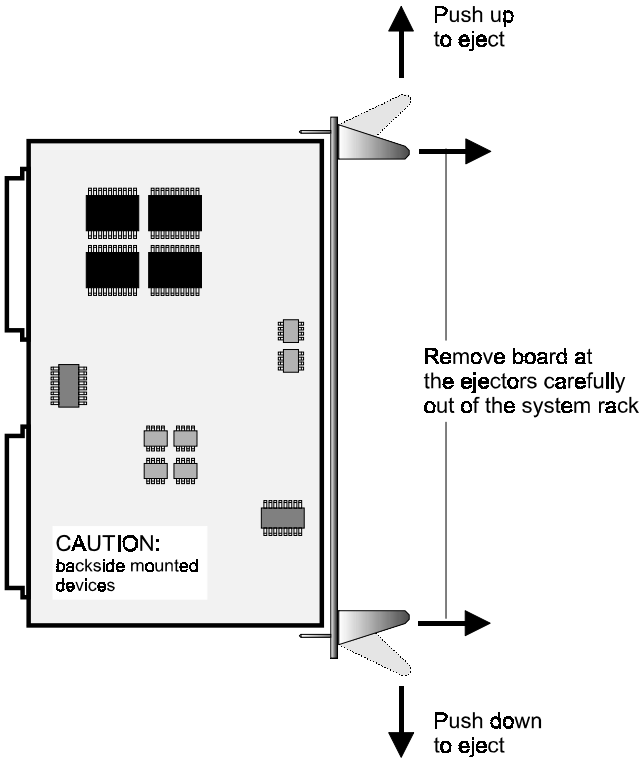
Removing boards

- Switch off the main power supply.
- Touch the system rack to guarantee electrostatic discharge.
- Optionally remove screws if board and rack are mounted together.
- Press the board out of the *CompactPCI* ® backplane by pushing the ejectors in the front panel apart each other (see illustration below).
- Move board carefully along the guide rails out of the rack. Caution is given especially to the devices mounted on the backside of the circuit board.
- Put the removed board in the original EKF packaging box.



Removing board from the system rack

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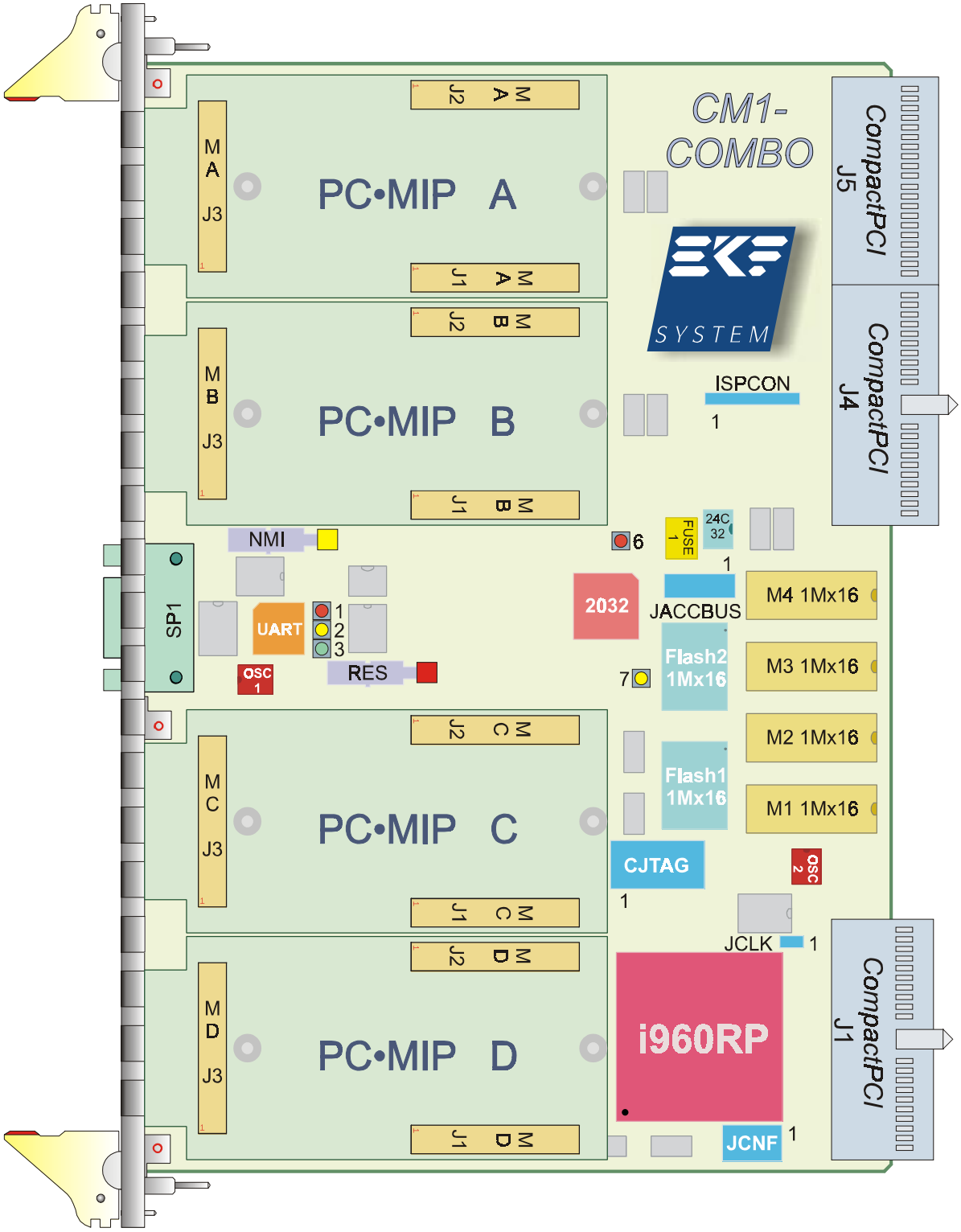
Connectors, Jumper Fields, Factory Defaults



Assembly Drawing

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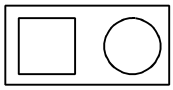
For the positions of the connectors and jumper fields see the assembly plan above.

Connectors

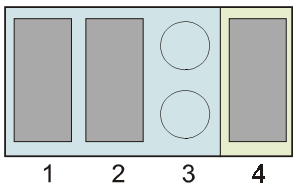
JACCBUS	ACCESS.bus / I^2C Interface (4-pin Header)
J1	*CompactPCI* ® Connector
J4	*CompactPCI* ® Connector (PC•MIP Module I/O)
J5	*CompactPCI* ® Connector (PC•MIP Module I/O)
MAJ1, MAJ2	PC•MIP PCI Interface Module A
MAJ3	PC•MIP I/O Interface Module A
MBJ1, MBJ2	PC•MIP PCI Interface Module B
MBJ3	PC•MIP I/O Interface Module B
MCJ1, MCJ2	PC•MIP PCI Interface Module C
MCJ3	PC•MIP I/O Interface Module C
MDJ1, MDJ2	PC•MIP PCI Interface Module D
MDJ3	PC•MIP I/O Interface Module D
SP1	RS-232 Serial Interface (DSub-9)

Jumper Field Factory Defaults



Factory
Default JCLK

Clock Source Selector:
Clock sourced from *CompactPCI* ® Bus Clock



Factory Default **JCNF**

i960®RP Configuration Selector:

1. Initialization Mode 0 (CPU held in reset)
2. Accept CPCI Configuration Cycles
3. BIST active
4. CPCI Reset Passed Through to Local Reset

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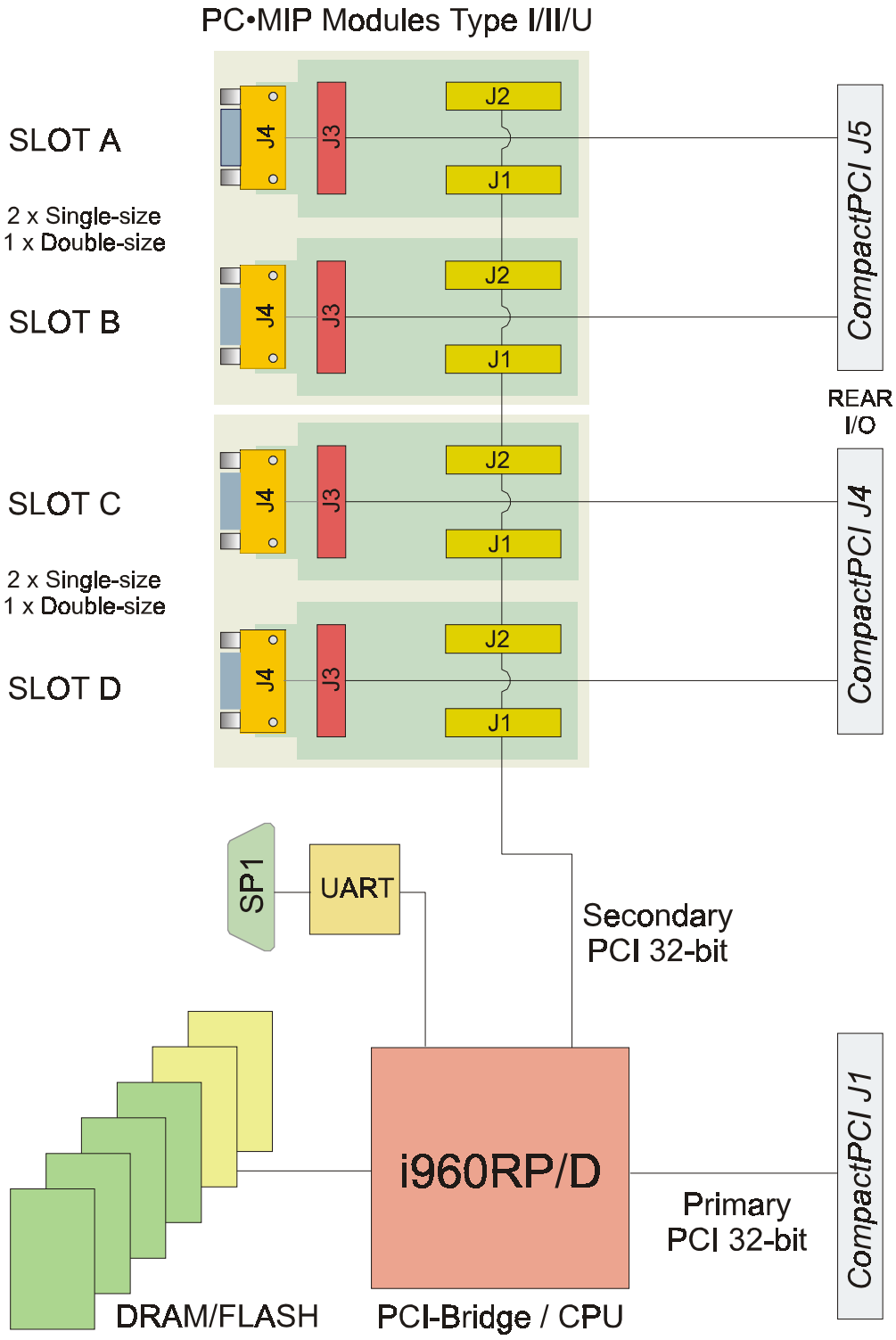
Block Diagram CM1-COMBO



Block Diagram CM1-COMBO

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i960®RP Processor

General Features

The central unit on the CM1-COMBO is an i960®RP I/O Processor, a member of the 80960 family of high performance processors. It combines a high-speed CPU with powerful features to create an intelligent I/O processor and integrates it into a Peripheral Components Interconnect (PCI) environment. This multi-function PCI device is fully compliant with the *PCI Local Bus Specification*, revision 2.1. The i960®RP local bus, a 32-bit multiplexed burst bus, is a high-speed interface to system memory and I/O. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs). The core can maintain a sustained execution rate of one instruction per clock of most instructions.

The i960®RP features include:

- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- 128-bit register bus speeds local register caching
- 4 Kbyte two-way, integrated instruction cache
- 2 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated, zero wait state data RAM
- PCI-to-PCI Bridge Unit
- Address Translation Unit
- DMA Controller
- Messaging Unit
- Memory Controller
- I^2C Bus Interface Unit

The PCI-to-PCI bridge provides a connection path between two independent 32-bit PCI buses and provides the ability to overcome PCI electrical loading limits. On the CM1-COMBO the bridge creates a data path between the *CompactPCI* ® bus and the PC•MIP modules. The bridge unit is fully compliant with the *PCI-to-PCI Bridge Architecture Specification*, revision 1.0 published by the PCI Special Interest Group. It allows certain bus transactions on one PCI bus to be forwarded to the other PCI bus. Dedicated data queues support high-performance bandwidth on the PCI buses. The i960®RP supports PCI 64-bit Dual Address Cycle (DAC) addressing. The bridge has dedicated PCI configuration space that is accessible through the primary PCI bus.

The two Address Translation Units (ATUs) permit direct data access from either PCI interface (***CompactPCI*** ® and PC•MIP) to local memory. This allows for example the programming of the FLASH devices or downloading software to local memory via the primary *CompactPCI* ® interface without interaction of the i960®RP core. Address translation is controlled through programmable, memory-mapped registers accessible from both the PCI interface and the i960 core processor. The primary ATU has a dedicated PCI configuration space that is accessible through the *CompactPCI* ® bus or the i960 core. The secondary PCI configuration space is accessible by the i960 core only.

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and i960®RP local memory. Three separate DMA channels accommodate data transfers: two for the *CompactPCI* ® bus, one for the secondary PCI bus. The DMA Controller supports chaining and unaligned data transfers.

The Messaging Unit (MU) provides data transfer between the PCI system and the i960®RP. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues and Index Registers. Each allows a host processor or external PCI device and the i960®RP to communicate through message passing and interrupt generation. The MU makes it easy to realize the Intelligent I/O Interface I_2O.

The Memory Controller allows direct control of the external memory respectively the memory-mapped I/Os on the CM1-COMBO, including DRAM, Flash EEPROM and the serial interface. It features programmable chip selects and a wait state generator. External memory can be configured as PCI addressable memory or private i960®RP memory.

Additional Documentation

A detailed description of these and other features including the programming of the i960 ®RP processor could be find in the documentation listed below. Electronic information can be obtained via

http://www.intel.com

i960®RP Related Documentation

Document Title	Order Number
i960®Rx I/O Microprocessor Developer's Manual	Intel Order # 272736
i960®Rx I/O Processor Specification Update	Intel Order # 272918
i960®RP/RD I/O Processor at 3.3 Volts data sheet	Intel Order # 273001
i960®Jx Microprocessor User's Guide	Intel Order # 272483

Clock and Reset Generation

Clock Generation

The CM1-COMBO is clocked by a single, 33 MHz signal. This master clock controls the entire timing of the i960®RP and is also the clock of the four PC•MIP module slots. The main clock input is fed by one of two possible sources, chosen by the 2x1 clock selection jumper **JCLK** near the **J1** connector on the CM1-COMBO:

Clock Selection Jumper JCLK Setting Options

Clock Source	JCLK
CompactPCI ® Bus Clock Signal (**J1** Pin D6)	removed
33 MHz Oscillator on the CM1-COMBO	set

Normally the CM1-COMBO will be integrated in a *CompactPCI* ® rack with a system controller and possibly other boards. In this case always the bus clock signal should be used as clock source (**JCLK** removed!).

To support a single stand-alone operation without system controller the CM1-COMBO provides an on-board 33 MHz oscillator that generates the necessary clock. When setting the jumper **JCLK** the oscillators output is connected to the clock input of the board.

CAUTION:
Note that in this case the clock signal also occurs on the clock pin of the *CompactPCI* ® connector **J1** (Pin D6). This will lead to clock signal crashing on the bus if more than one board drives the clock.

The clock signal is distributed on the CM1-COMBO via a dedicated clock buffer to provide a low skew, well conditioned signal as required by the PCI specification.

Power-On and Manual Reset

There are a lot of reasons which trigger a reset on the CM1-COMBO:

(1) Power-On (switching on the power supply)
(2) V_{cc5} drops below 4.65V (power failed)
(3) V_{cc3} drops below 3.0V (power failed)
(4) Triggering the *CompactPCI* ® reset signal (**J1** Pin C5, **JCNF**(4) on)
(5) Reaching time out of the hardware watchdog
(6) Software reset caused by the i960®RP processor

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The first 5 sources will reset all devices on the CM1-COMBO to a known state. An integrated power supervisor generates a clean reset signal with a minimum length of 140 ms even if the voltages haven't stabilized at power-on. The signal is fed to the i960®RP, the Flash EEPROMs, the serial controller 16C550 and the four PC•MIP module slots. The processor can reset all four PC•MIP modules by asserting the secondary PCI bus reset in the Bridge Control Register (BCR, bit 6).

Further it can reset the 16C550 by triggering the local bus reset signal in the Extended Bridge Control Register (EBCR, bit 5). The i960 core is not able to reset the Flash EEPROMs.

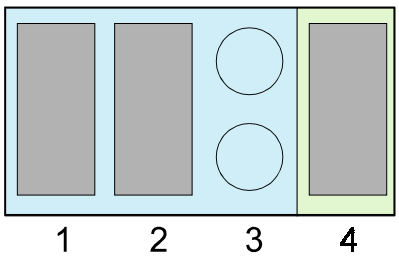
Hardware Watchdog

The CM1-COMBO is equipped with a hardware watchdog. The watchdog is disabled after a hardware reset. It is activated by toggling the general purpose output OUT1# of the UART. This is done by changing bit 2 in the Modem Control Register MCR of the UART (see section *RS-232 Serial Interface* for details of the UART's registers).

If the processor once touched MCR(2), the watchdog is armed and must be triggered at least every 1000 ms. A hardware reset will occur after a maximum time of 1.6 sec after the last watchdog trigger pulse.

i960®RP Initialization Modes

The behavior of the i960®RP after reset is controlled by the configuration selection jumper field JCNF. The processor supports four initialization modes 0 to 3, where mode 1 makes no sense on the CM1-COMBO.



Jumper Field JCNF

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Configuration Jumper Field JCNF Initialization Mode Setting Options

Initialization Mode	JCNF 1	JCNF 2	*CompactPCI* ® Interface	i960RP core processor
Mode 0	set	set	accepts transactions	held in reset
Mode 1 [1])	set	removed	retries all config. transactions	held in reset
Mode 2	removed	set	accepts transactions	initializes
Mode 3	removed	removed	retries all config. transactions	initializes

[1]) Not useful on the CM1-COMBO

Mode 0 allows a host processor to configure the i960®RP peripherals while the i960 core processor is held in reset. The host processor configures the PCI-to-PCI bridge by assigning bus numbers, allocating PCI address space, and assigning IRQ numbers. The memory controller and ATU can also be initialized by the host processor. Program code for the i960 core processor may be downloaded into local DRAM or Flash EEPROM by the host processor. The host processor then clears the i960 reset signal by clearing the Core Processor Reset bit in the Extended Bridge Control Register (EBCR, bit 1). This deasserts the internal reset signal on the i960 core processor and the processor begins its initialization process.

Mode 2 allows configuration cycles on the PCI-to-PCI bridge at any time and allows the i960 core processor to initialize after reset. Mode 2 allows each unit of the i960®RP to be initialized in its own manner. Be aware that race conditions may exist between i960 core operation after reset and host processor PCI configuration.

Mode 3 allows the i960 core processor to initialize and control the initialization process before the host processor is allowed to configure the i960®RP peripherals. During this time, the *CompactPCI* ® interface signals a Retry on all configuration cycles it receives until the i960 core processor clears the Configuration Cycle Disable bit in the EBCR.

The 3rd jumper of JCNF exists to enable or disable the i960®RP's build-in self test (BIST). If enabled the processor tries to check all its internal units. If the check failed the processor asserts a signal that lights the red on-board LED CPU FAIL and core execution stops. Because BIST needs about 414000 CPU cycles it may be necessary to disable it when the restart time needs to be minimized.

Configuration Jumper Field JCNF BIST Setting Options

JCNF 3	Processor BIST
removed	enabled
set	disabled

Jumper 4 of JCNF is used to forward the reset signal from the *CompactPCI* ® bus to the CPU and the other local devices on the board.

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Configuration Jumper Field JCNF CPCI Reset Setting Options

JCNF 4	CPCI Reset
removed	ignored
set	forwarded to the board

It is a good idea to remove JCNF 4 when the BIOS of the main CPU board within the *CompactPCI* ® does not recognize the CM1-COMBO after system reset.

Local Devices

Flash EEPROM

The CM1-COMBO is equipped with on-board programmable Flash EEPROM devices. The data bus width to these devices is 32-bit allowing the i960®RP to execute program code from Flash in full speed. Therefore it is not necessary to copy the code into DRAM. The Flash devices are connected to the memory bank 0 of the i960®RP Memory Controller. They are readable and especially writeable any time with no need to enable the programming voltage. Caution is given when the processor itself tries to program the Flash devices while executing code from the Flashs. This will lead to a hanging processor core. To program the Flash devices use one of the following alternates:

1. Programming by i960®RP core processor: Copy the program data and the Flash programming algorithm code to DRAM. Run the programming code from DRAM. Return to the calling function or restart the code loaded into the Flash devices.

2. Programming via *CompactPCI* ® interface: Reset the CM1-COMBO with JCNF setting to initialization mode 0. Alternatively the i960®RP core processor could be halted by executing the HALT instruction. Program the Flash devices via the primary ATU. Restart the processor.

Depending on the version of the CM1-COMBO there are different types of Flash devices in use:

- 28F016SV / Intel
- 28F160S5 / Intel

These devices distinguish in access times and programming algorithms. Programming tools (currently running on LINUX or WinXX) are offered by EKF and are available on request. The following table shows the necessary initializations in the read and write wait state registers (MBRWS0, MBWWS0) of the i960®RP memory controller dependent on the devices in use. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

Flash Device Read And Write Wait State Settings

Flash Device	Read		Write	
	Access [ns]	MBRWS0	Access [ns]	MBWWS0
28F016SV	70	0x00000220	70	0x00000221
28F160S5	70	0x00000220	70	0x00000220

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Dynamic Random Access Memory (DRAM)

The CM1-COMBO offers a working memory space of 8 Mbyte. The memory is organized in two banks of non-interleaved DRAM, each 4 Mbyte in size. The data path width is 32-bit without parity. Similar to the Flash EEPROMs different types of DRAM devices are in use. Possible types are

- Fast Page Mode (FPM) DRAMs
- Extended Data Out (EDO) DRAMs

with an access time of at least 70 ns. The following table shows typical values to program to the i960®RP memory controller to setup the DRAM interface. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

DRAM Initialization Parameters

Name	Register	Value	Description
DRWS	DRAM Bank Read Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DWWS	DRAM Bank Write Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DRIR	DRAM Refresh Interval	0x00010204	Refresh enabled, 15.625 µs refresh interval
DPER	DRAM Parity Enable	0x00000000	DRAM parity disabled
DBCR	DRAM Bank Control	0x0000000D 0x0000004D	High-current drives disabled, DRAM bank enables, Fast Page Mode (FPM), 2 banks or Extended Data Out (EDO), 2 banks

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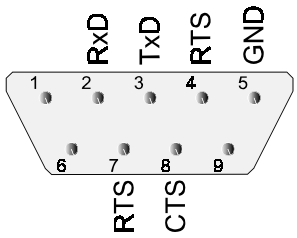
RS-232 Serial Interface

To connect the CM1-COMBO to different peripheral devices the board offers a RS-232 serial interface. The serial signals are fed to the male DSub-9 connector SP1 in the front panel (labeled as RS232) of the board. This allows to make a simple link to serial interfaces of terminals, personal computers etc.



Connector SP1

The above illustration shows the pin assignments to the connector SP1 (front view of the connector). Signal directions are seen from the view of the CM1-COMBO, e.g. RxD (SP1, pin 2) is an input to the CM1-COMBO. Unnamed pins are not connected to any signal on the board. The handshake input CTS (SP1, pin 8) is pulled up by a resistor to bring the line to a proper state if the handshake signals are not used. The pins 4 and 7 are pulled together on the board to the RTS line.

The interface is based on the well known Asynchronous Communication Element (ACE) 16C550. Clocked with a seperate 14.7456 MHz oscillator a transfer rate of up to 921.6 KBaud is possible. The ACE is connected to bank 1 of the i960®RP's memory controller. The following table shows the addressing of the ACE's registers relative to its base address:

ACE (16C550) Register Offset Definitions

Base Address Offset	Read Access	Write Access
0x00	Receiver Buffer Register (**RBR**)	Transmitter Holding Register (**THR**)
0x04	Interrupt Enable Register (**IER**)	Interrupt Enable Register (**IER**)
0x08	Interrupt Ident. Register (**IIR**)	FIFO Control Register (**FCR**)
0x0C	Line Control Register (**LCR**)	Line Control Register (**LCR**)
0x10	Modem Control Register (**MCR**)	Modem Control Register (**MCR**)
0x14	Line Status Register (**LSR**)	not allowed
0x18	Modem Status Register (**MSR**)	ignored
0x1C	Scratch Register (**SCR**)	Scratch Register (**SCR**)

In order to get a proper function of the ACE, the following values should be programmed to the wait state registers of memory bank 1. Burst accesses to the ACE are **not** allowed.

ACE (16C550) Read And Write Wait State Settings

MBRWS1	MBWWS1
0x00000302	0x00000302

The ACE is able to request i960®RP core interrupts. The request line of the ACE is fed to the interrupt input XINT5# of the processor. An IRQ can be identified by checking the IIR of the ACE in the interrupt service routine. The request is released by accessing the corresponding register that caused the interrupt (e.g. reading an incoming character from the RBR). See ACE data sheets and i960®RP manual for detailed description of interrupt programming.

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I²C Interface

The i960®RP supports a master and slave interface to the popular I²C (Inter-Integrated Circuit) bus. This simple, two wire serial bus allows an easy connection to other I²C devices. Transfer rates of up to 400 Kbit/s are possible. It could be programmed via the I²C unit registers of the i960®RP.

An I²C message consists of a device addressing byte and additional data bytes. The device address byte also contains the information wether the following operations are read or write transfers. If the address of an I²C slave device on the bus matches the device address byte sent by a master, the slave acknowledges the transfer.

General I²C Addressing Byte Format

A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W
MSB							LSB

On write operations (R/W=0) the master may send then further data bytes to the slave until the master generates a stop condition. Each byte transferred is acknowledged by the recipient. Read operations are working in the same way except that R/W=1 and that the data flow is reversed.

Serial EEPROM 24C32

The CM1-COMBO offers a serial EEPROM 24C32 with a capacity of 4 Kbytes. This device can be used e.g. to permanently store important parameters that should be non volatile even if the power disappears. It is accessible as slave device via the I²C bus. Write accesses to the memory array of the serial EEPROM are possible any time because the hardware write protection feature of the 24C32 is not enabled on CM1-COMBO.

Serial EEPROM 24C32 Addressing Byte Format

1	0	1	0	0	0	0	R/W
MSB				A_2	A_1	A_0	LSB

The above figure shows the I²C bus device addressing byte that must be written to the serial EEPROM in order to read (R/W=1: DeviceAddr=0xA1) or write (R/W=0: DeviceAddr=0xA0) data from or to it (the 3 external address lines A_{2-0} offered by the 24C32 are hard-wired to GND on the CM1-COMBO). Read and write accesses with the I²C bus maximum speed of 400 Kbit/s are supported by the device.

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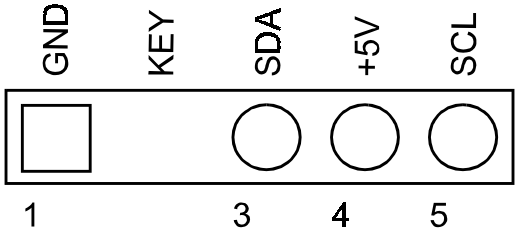
ACCESS.bus Interface

To make it easy to connect external I^2C devices to the CM1-COMBO the board offers an ACCESS.bus interface via the 4-pin connector **JACCBUS**. The ACCESS.bus is similar to the System Management Bus (SMBus) based on the I^2C bus. Both standards are compatible to the I^2C bus with exception of a few electrically (e.g. max. load capacity) and mechanical (e.g. ACCESS.bus defines a connector, I^2C does not) specifications.

The ACCESS.bus interface on the CM1-COMBO supports up to 126 devices (7-bit device addresses minus the broadcast address and the on-board serial EEPROM) over a total cable length of 8 m with a maximum data rate of 100 Kbit/s. Each device may use its own data rate. The cable consists of two shielded pairs: a Ground/+5V pair and a clock/data pair.



Connector JACCBUS

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Interrupts

The i960®RP provides an on-chip programmable interrupt controller that allows a flexible, priority level based reaction to internal and external events. The processor uses interrupt vector numbers to enter the interrupt service routine (ISR). This mechanism leads to fast reaction and low interrupt latency. To optimize interrupt performance the vectors can be hold in the i960®RP internal RAM and the ISR can be frozen in the instruction cache. See the i960®RP manual for details.

Internal interrupt events have their origin by the different units within the i960®RP like the I^2C unit, the messaging unit etc. External requests are fed to the processor via 8 maskable (XINT0#...XINT7#) and one non-maskable (NMI#) interrupt inputs. The four inputs XINT0#...XINT3# are shared with the secondary (PC•MIP) PCI interrupt inputs S_INTA#...S_INTD#. Four bits within the PCI interrupt routing select register (PIRSR) decide for each XINT#/S_INT#-pin wether the interrupt is lead to the i960 core or to the *CompactPCI* ® interface.

The CM1-COMBO owns the following peripheral interrupt devices:

(1) the four PC•MIP modules via S_INTA#...S_INTD#
(2) the serial controller ACE via XINT5#
(3) the NMI push button via NMI# (non-maskable!)

For a description of the first two sources refer to the corresponding chapters.

The NMI push button is a nice tool when debugging software on the CM1-COMBO. A debugger can enter the control of a running program when pushing the NMI push button. Because this interrupt can not be masked by a program, getting program control is always possible. The interrupt request of the NMI button is active while the button is pushed. It can be identified by checking the NMI interrupt status register (NISR, bit 8).

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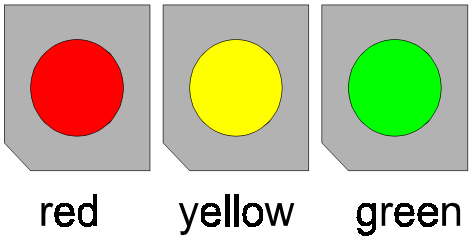
Diagnostics Display

There are three LEDs on the CM1-COMBO indicating the current state of the board. Since no space was available **in the front panel** the LEDs are mounted near the back side of the **SP1** connector. They are visible through one of the PC•MIP module windows in the front panel.



Diagnostics Display

The LEDs are having the following meaning:

Diagnostics Display Information

LED	lighten	not lighten
red (core state)	build-in self test failed, or local bus confidence test failed, or processor held in reset state: core execution stopped	both build-in self test and local bus confidence test passed: core is in executing mode
yellow (PC•MIP access)	access to one of the PC•MIP modules	no access to any of the PC•MIP modules
green (local access)	access to local DRAM, Flash or ACE	no access to any local device

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CompactPCI ® Interface

The CM1-COMBO offers a CompactPCI ® interface complying to the CompactPCI ® *Specification Revision 2.1*. CompactPCI ® is an industrial implementation of the familiar *Peripheral Component Interconnect* (PCI) bus. It combines the well known electrical features of PCI with the more robust mechanical 19 inch rack mounting technology. The interface supports 64-bit address and 32-bit data transfers. It is designed for a clock frequency of 33 MHz with a transfer rate of up to 132 Mbyte/s.

PCI Devices

The CompactPCI ® interface is realized by the i960® RP processor. It consists of two PCI functions, thus it is a multi-function PCI device. The first function (PCI function 0) is the PCI-to-PCI bridge unit which creates a data path between the primary (the CompactPCI ®) and the secondary (the PC•MIP) interface. PCI function 1 is the primary Address Translation Unit (ATU). This unit allows high-speed accesses from the CompactPCI ® interface to the local bus devices like Flash EEPROM or DRAM. Normally a BIOS running on a host system detects these PCI devices at boot time.

PCI-To-PCI Bridge Unit

The PCI-to-PCI bridge unit serves as an electrical and logical buffer helping to overcome the electrical limits of the PCI bus. Its main function is to provide a data path between the two independent PCI buses of the CompactPCI ® and the PC•MIP interface. The bridge unit features full compliance to the *PCI-to-PCI Bridge Architecture Specification*, revision 1.0. It supports both upstreaming (from CompactPCI ® to PC•MIP) and downstreaming (from PC•MIP to CompactPCI ®) transfers. Six 64-byte posting buffers are implemented in the bridge unit, three for each direction.

PCI offers three separate address spaces:

- 4 Gbyte memory address space
- 64 Kbyte I/O address space (16-bit addressing)
- 256 Byte configuration space

The bridge unit acts as a filter between the primary and secondary interfaces. When a memory or I/O address is falling in the address window programmed in the bridge's configuration space this transaction is forwarded to the other PCI interface.

The configuration space of the bridge is accessible by the i960 core via memory mapped registers starting at local address 0x1000. Alternative a host can access it via CompactPCI ® type 0 configuration read or write cycles to PCI function number zero. Some registers are read-only by type 0 accesses but writable by the i960 core. This allows to processor to initialize the bridge unit before the configuration process begins. The following table shows the structure of the configuration space:

Bridge Configuration Header Format

Bridge Configuration Header				Address Offset
Device ID		Vendor ID		0x00
Primary Status		Primary Command		0x04
Class Code			Revision ID	0x08
Reserved	Header Type	Primary Latency Timer	Cacheline Size	0x0C
Reserved				0x10
				0x14
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	0x18
Secondary Status		I/O Limit	I/O Base	0x1C
Memory Limit		Memory Base		0x20
Prefetchable Memory Limit		Prefetchable Memory Base		0x24
Reserved				0x28
				0x2C
				0x30
Subsystem ID		Subsystem Vendor ID		0x34
Reserved				0x38
Bridge Control		Reserved		0x3C
Secondary IDSEL Control		Extended Bridge Control		0x40
Primary Bridge Interrupt Status				0x44
Secondary Bridge Interrupt Status				0x48
Secondary Arbitration Control				0x4C
PCI Interrupt Routing Control				0x50
Reserved		Secondary I/O Limit	Secondary I/O Base	0x54
Secondary Memory Limit		Secondary Memory Base		0x58
Reserved		Secondary Decode Enable		0x5C

The registers with offset 0 to 0x38 are standard PCI-to-PCI bridge registers, while the registers from 0x3C to 0x5C are i960®RP specific. See i960®RP manual for details of the registers meaning.

Address Translation Unit (ATU)

The Address Translation Unit (ATU) provides an interface between the *CompactPCI* ® or PC•MIP buses and the i960 local bus. It consists of two parts: the primary ATU for accesses from *CompactPCI* ® and the secondary ATU for accesses from the PC•MIP modules. Data transfers initiated by any PCI bus master to a local bus device are called *inbound* transactions. If the i960 core starts a data access to any PCI bus slave, this is called an *outbound* transfer.

The ATUs fulfil both address filtering and address translation. For inbound transactions an ATU uses three registers:

- Inbound ATU Base Register
- Inbound ATU Limit Register
- Inbound ATU Translate Value Register

A PCI address is detected as an inbound transaction by the ATU if

(PCI_Address & Limit_Register) == Base_Register.

The incoming 32-bit PCI_Address is bitwise ANDed with the Limit_Register. When the result matches the Base_Register, the PCI_Address is detected as being within the inbound translation window. This opens a PCI address window from (Base_Register) to (Base_Register + Limit_Register). Once the transaction is claimed, the address must be translated from a 32-bit PCI address to a 32-bit local address. For that the incoming PCI_Address is first bitwise ANDed with the bitwise inverse of the Limit_Register. This result is bitwise ORed with the ATU Translate_Value_Register. The result is the 32-bit local address:

Local_Address = (PCI_Address & (~Limit_Register)) | Translate_Value_Register

In addition the ATUs provide address detection and translation for i960 core processor-initiated cycles targeted to one of the PCI buses. Both ATUs support two different translation modes:

- Address Translation Windows
- Direct Addressing Window

The address translation windows are located from 0x8000 0000 to 0x9001 FFFF within the 32-bit local address space of i960 processor. This range consists of two 128 Mbyte memory windows and two 64 Kbyte I/O windows for the primary and secondary ATU respectively. Each memory window is divided into two areas, 64 Mbyte for 32-bit PCI address cycles and 64 Mbyte for PCI double address cycles (DAC). The type of the PCI transfer is dependent from the area that is hit within the address translation window by the i960 core.

The translation mechanism used is very similar to the algorithm for the inbound transactions described above. For memory and DAC accesses it is

PCI_Address = (Local_Address & 0x03FF FFFF) | Memory_Window_Value_Register

I/O transactions are translated by

PCI_Address = (Local_Address & 0x0000 FFFF) | I/O_Window_Value_Register

In addition the i960®RP provides a direct addressing scheme. This method of outbound PCI transactions is limited to memory transfers and works within the local address range from 0x0000 2000 to 0x7FFF FFFF only. If enabled any access to these locations are forwarded to the PCI bus. Which of the PCI buses are used will be decided by a bit in the ATU control register ATUCR. This register also contains the direct addressing enable bit.

As every PCI device the ATUs implements their own configuration space. This space is 256 bytes in size, whereas the first 64 bytes must adhere to a predefined header format. Primary and secondary ATU are programmed via type 0 configuration commands on the primary interface to PCI function number one. Besides the i960 core processor can access the configuration space via memory mapped registers at local address 0x1200. Some of the read-only registers can also be written by the i960. The following table shows the configuration header according the *PCI Local Bus Specification*, revision 2.1:

Address Translation Unit Configuration Header Format

<table>
<tr><th colspan="4">Address Translation Unit Configuration Header</th><th>Address Offset</th></tr>
<tr><td colspan="2">ATU Device ID</td><td colspan="2">ATU Vendor ID</td><td>0x00</td></tr>
<tr><td colspan="2">ATU Primary Status</td><td colspan="2">ATU Primary Command</td><td>0x04</td></tr>
<tr><td colspan="3">ATU Class Code</td><td>ATU Revision ID</td><td>0x08</td></tr>
<tr><td>BIST</td><td>Header Type</td><td>Latency Timer</td><td>Cacheline Size</td><td>0x0C</td></tr>
<tr><td colspan="4">Primary Inbound ATU Base Address</td><td>0x10</td></tr>
<tr><td colspan="4" rowspan="5">Reserved</td><td>0x14</td></tr>
<tr><td>0x18</td></tr>
<tr><td>0x1C</td></tr>
<tr><td>0x20</td></tr>
<tr><td>0x24</td></tr>
<tr><td colspan="2">ATU Subsystem ID</td><td colspan="2">ATU Subsystem Vendor ID</td><td>0x28
0x2C</td></tr>
<tr><td colspan="4">Expansion ROM Base Address</td><td>0x30</td></tr>
<tr><td colspan="4" rowspan="2">Reserved</td><td>0x34</td></tr>
<tr><td>0x38</td></tr>
<tr><td>Max. Latency</td><td>Minimum Grant</td><td>Interrupt Pin</td><td>Interrupt Line</td><td>0x3C</td></tr>
</table>

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The next table shows the i960®RP specific registers of the ATU configuration space.

ATU Extended PCI Configuration Register Space		Address Offset
Primary Inbound ATU Limit Register PIALR		0x40
Primary Inbound ATU Translate Value Register PIATVR		0x44
Secondary Inbound ATU Base Address Register SIABAR		0x48
Secondary Inbound ATU Limit Register SIALR		0x4C
Secondary Inbound ATU Translate Value Register SIATVR		0x50
Primary Outbound Memory Window Value Register POMWVR		0x54
Reserved		0x58
Primary Outbound I/O Window Value Register POIOWVR		0x5C
Primary Outbound DAC Window Value Register PODWVR		0x60
Primary Outbound Upper 64-bit DAC Register POUDR		0x64
Secondary Outbound Memory Window Value Register SOMWVR		0x68
Secondary Outbound I/O Window Value Register SOIOWVR		0x6C
Reserved		0x70
Expansion ROM Base Address Register ERBAR		0x74
Expansion ROM Translate Value Register ERTVR		0x78
Reserved		0x7C
		0x80
		0x84
ATU Configuration Register ATUCR		0x88
Reserved		0x8C
Primary ATU Interrupt Status Register PATUISR		0x90
Secondary ATU Interrupt Status Register SATUISR		0x94
Secondary ATU Status Register	Secondary ATU Commond Register	0x98
Secondary Outbound DAC Window Value Register SODWVR		0x9C
Secondary Outbound Upper 64-bit DAC Register SOUDR		0xA0
Primary Outbound Configuration Cycle Address Register POCCAR		0xA4
Secondary Outbound Configuration Cycle Address Register SOCCAR		0xA8
Primary Outbound Configuration Cycle Data Register POCCDR		0xAC
Secondary Outbound Configuration Cycle Data Register SOCDCR		0xB0
Reserved		0xB4 - 0xFF

System Connector J1/P1

The *CompactPCI* ® specification defines the usage of shielded, 2 mm-pitch, 5-row connectors on *CompactPCI* ® boards according to IEC 917 and IEC 1076-4-101. The 32-bit PCI interface is implemented via the J1/P1 connector, while the 64-bit option requires the connector J2/P2. Since the CM1-COMBO has a 32-bit *CompactPCI* ® interface the J2/P2 connector is not necessary and thus not mounted.

The J1/P1 connector also defines the supported signaling voltage ($V_{I/O}$). A coding key in this connector is used to distinguish boards with $V_{I/O}$ = 3.3 V (cadmium yellow key), $V_{I/O}$ = 5 V (brilliant blue key) or both (no key). The CM1-COMBO is laid out for $V_{I/O}$ = 5 V only and equipped with a blue coding key.

CAUTION:

Do not use the CM1-COMBO within a 3.3 V *CompactPCI* ® system.

***CompactPCI* Connector J1 Pin Assignment**

#J1	A	B	C	D	E
25	5V	REQ64# [1])	ENUM# [1])	3.3V	5V
24	AD1	5V	VI/O	AD0	ACK64# [1])
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN [2])	C/BE0#
20	AD12	GND	VI/O	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR#	GND	3.3V	PAR	C/BE1#
17	3.3V	SDONE [1])	SBO# [1])	GND	PERR#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	GND	TRDY#
14	Coding Key Area (Brilliant Blue)				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	IDSEL	AD23	GND	AD22

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8	AD26	GND	VI/O	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ#	GND	3.3V	CLK	AD31
5	BRSVP1A5 [1])	BRSVP1B5 [1])	RST#	GND	GNT#
4	BRSVP1A4 [1])	GND	VI/O	INTP [1])	INTS [1])
3	INTA#	INTB#	INTC#	5V	INTD#
2	TCK	5V	TMS	TDO	TDI
1	5V	-12V	TRST#	+12V	5V
#J1	**A**	**B**	**C**	**D**	**E**

Notes:
[1]) These pin positions are not connected on the CM1-COMBO.
[2]) This signal is hardwired to GND on the CM1-COMBO.

I/O Connectors J4/P4 and J5/P5

The CM1-COMBO uses the *CompactPCI* ® connectors J4/P4 and J5/P5 to pass the I/O signals of the PC•MIP modules to the rear of the system rack. See Chapter *PC•MIP Module Slots* for details of pin assignments.

PC•MIP Module Slots

The PC•MIP module concept was designed to offer flexible I/O solutions at moderate costs. This was reached by combining the advantages of PCI, the good experiences of other module concepts like *PCM* or *M-Module* and a small module dimension.

The PC•MIP module standard is currently under development by the VITA-29 Task group of ANSI/VITA (Draft Standard Revision 0.93, February 1, 2001). Information can be obtained by

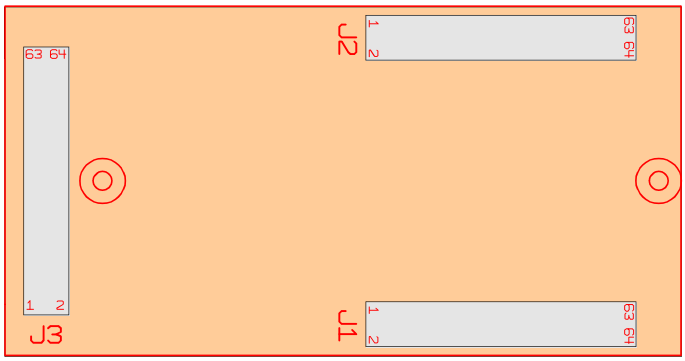
VITA Standards Organization
7825 East Gelding Drive, Suite 104
Scottsdale, AZ 85260
USA
++1 (602) 951-8866
www.vita.com

Module Types

To adapt to different applications two basic types of PC•MIP modules are defined:

- Type I modules use the J3 connector of the module to pass I/O signals to the CM1-COMBO for rear panel I/O,
- Type II modules use an integral I/O connector for I/O via the front panel of the CM1-COMBO.

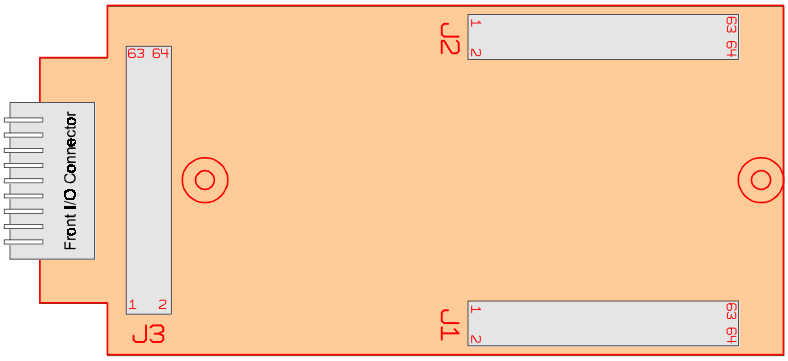
In addition the PC•MIP specification distinguishes single-size modules and double-size modules. The following schematic figure shows the general appearance of a single-size type I module.



Single-size PC•MIP Type I Module

Type I modules are 47 mm by 90 mm in size. They route their I/O signals to the J3 connector of the module and then via traces on the CM1-COMBO to the *CompactPCI* ® connectors J4/P4 or

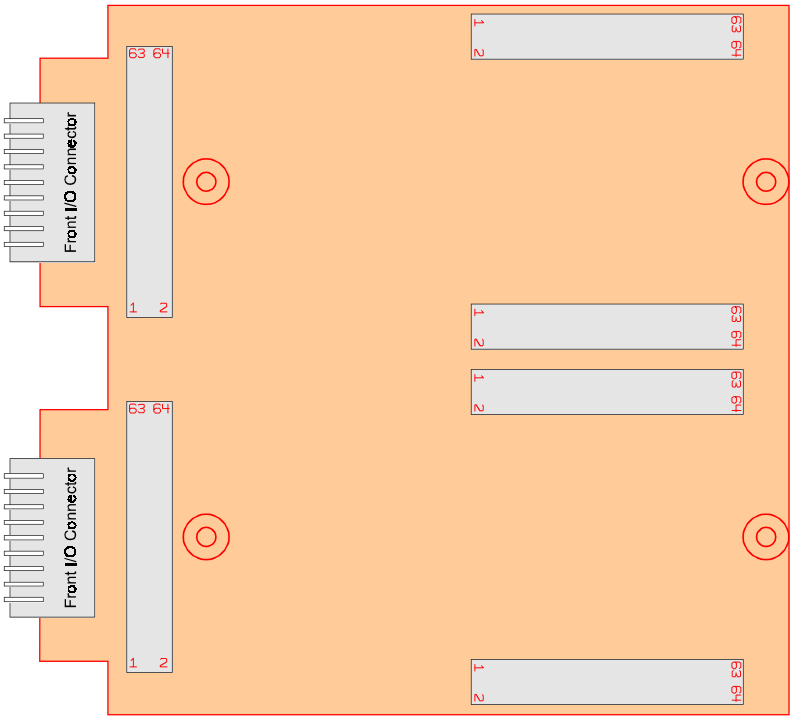
J5/P5. This kind of I/O wiring makes it easy to remove the CM1-COMBO from the system rack with no need to remove any cable before.



Single-size PC•MIP Type II Module

Type II modules provide a porch where a dedicated I/O connector is located. The PC•MIP specification does not define a special type of connector to use. This allows putting I/O signals direct to the front panel of the CM1-COMBO and makes PC•MIP modules usable also for high-speed applications like Fast-Ethernet etc., that doesn't tolerate I/O wiring to the back-side of system rack. Nevertheless, a type II module always contains the J3 connector. J3 may be used by the module to get I/Os also on the rear of the system rack, but it doesn't have to do it. Type II modules have a nominal size of 47 mm by 99 mm.

Double-size modules are nearly twice the size of their single-size counterparts. Their sizes are 94.5 mm by 90 mm for type I and 94.5 mm by 99 mm for type II modules.



Double-size PC•MIP Type II Module

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The CM1-COMBO is capable to carry four single-size type I or type II modules on the landing zones **PC-MIP A**, **PC-MIP B**, **PC-MIP C** and **PC-MIP D**. The neighboring slots **PC-MIP A** / **PC-MIP B** and **PC-MIP C** / **PC-MIP D** respectively can carry double-size modules of any type.

Module Injector/Ejector

To simplify the installation and removing of a module PC•MIP uses an injector/ejector system. This consists of two **mounting standoffs** on the CM1-COMBO and two **captive screws** located at each end of the module. This construction offers the advantage, that the screws are used to fasten the module on the carrier board and in addition that the screws push the module out of the connectors when loosen the connection.

To install a module put the module loose on the PC•MIP slot and fix the two screws by turning them clockwise. This will pull the module connectors in the corresponding receptacle of the CM1-COMBO and fasten it.

Remove a module by turning the ejector screws counterclockwise. This will pushing the module out of the connectors until it could be taken off.

PCI Interface

The system interface of a PC•MIP module to its carrier board is based on PCI. PC•MIP modules are 100% compatible to the PCI standard defined by the *PCI Local Bus Specification*, revision 2.1. The modules are direct accessible by the i960 core processor via the secondary ATU and by a host via the PCI-to-PCI bridge unit within the i960®RP processor (see chapter *i960®RP Processor* for details).

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PCI IDSEL Assignment

Every PCI device provides a configuration space of 256 bytes. This space must be unique within the PCI system to configure each PCI device separately. To do so the PCI signal **IDSEL** of each module slot is connected to a different address line of the secondary PCI bus. The next table shows the corresponding assignment.

PC•MIP Module Slot IDSEL Assignment

PC•MIP Module Slot	IDSEL connected to address line
A	AD31
B	AD30
C	AD29
D	AD28

Access to the configuration space of a PC•MIP module is granted either by using the various types of PCI-to-PCI bridge configuration commands as defined by the PCI specification or by the i960 core processor via the secondary ATU. In the latter case the processor has to write the PCI configuration address to the Secondary Outbound Configuration Cycle Address Register (SOCCAR) first (see *PCI Local Bus Specification*, revision 2.1 for details on configuration address formats). The configuration data can then be written or read via the Secondary Outbound Configuration Cycle Data Register (SOCCDR).

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PCI Interrupt Routing

Each PC•MIP module slot offers the four interrupt request pins INTA#, INTB#, INTC# and INTD#. These signals are wired between two module slots using a rotating schema similar to the logical interrupt assignment defined by the *CompactPCI* ® specification. Assuming that each module drives just its INTA# pin this leads to a distributed interrupt request line load. On the CM1-COMBO with four slots no module has to share an INTx# signal with another one. The next table shows the assignments of the INTx# lines to the i960®RP PCI interrupt inputs. For example INTA# of slot A is connected to the i960's interrupt request input INTD#.

PC•MIP Interrupt Line Assignment

i960®RP	PC•MIP Slot A	PC•MIP Slot B	PC•MIP Slot C	PC•MIP Slot D
INTA#	INTB#	INTC#	INTD#	INTA#
INTB#	INTC#	INTD#	INTA#	INTB#
INTC#	INTD#	INTA#	INTB#	INTC#
INTD#	INTA#	INTB#	INTC#	INTD#

Connectors

PC•MIP modules are connected to the carrier board via three identical 64-pin connectors. These metric connectors have a pin spacing of 1 mm. The connectors MxJ1 and MxJ2 are used to provide the signals for the PCI system interface, while MxJ3 is the connector to wire the I/O signals to the rear-panel.

System Connectors MAJ1 ... MDJ1

The following table shows the pin assignment of the PC•MIP connectors MAJ1, MBJ1, MCJ1 and MDJ1 for the module slots A to D respectively.

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PC•MIP Connectors MAJ1 ... MDJ1 Pin Assignment

J1/P1 Pin	Signal Name	Signal Name	J1/P1 Pin
1	Reserved [1])	Reserved [1])	2
3	Reserved [1])	Reserved [1])	4
5	-12V	TRST#	6
7	TCK	+12V	8
9	GND	TMS	10
11	TDO	TDI	12
13	+5V	+5V	14
15	+5V	INTA# [2])	16
17	INTB# [2])	INTC# [2])	18
19	INTD# [2])	+5V	20
21	PRSNT1# [3])	Reserved [1])	22
23	Reserved [1])	+3.3V	24
25	PRSNT2# [3])	Reserved [1])	26
27	GND	GND	28
29	Reserved [1])	Reserved [1])	30
31	GND	RST#	32
33	CLK	+3.3V	34
35	GND	GNT#	36
37	REQ#	GND	38
39	+3.3V	Reserved [1])	40
41	AD31	AD30	42
43	AD29	+3.3V	44
45	GND	AD28	46
47	AD27	AD26	48
49	AD25	GND	50
51	+3.3V	AD24	52
53	C/BE3#	IDSEL [4])	54
55	AD23	+3.3V	56
57	GND	AD22	58
59	AD21	AD20	60
61	AD19	GND	62
63	+3.3V	AD18	64
J1/P1 Pin	**Signal Name**	**Signal Name**	**J1/P1 Pin**

Notes:
[1]) These pin positions are reserved by the PC•MIP specification and not connected.
[2]) See *PC•MIP Interrupt Line Assignment* table above for actual assignment.
[3]) These pin positions are not connected on the CM1-COMBO.
[4]) See *PC•MIP Module Slot IDSEL Assignment* table above for actual assignment.

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System Connectors MAJ2 ... MDJ2

The following table shows the pin assignment of the PC•MIP connectors MAJ2, MBJ2, MCJ2 and MDJ2 for the module slots A to D respectively.

PC•MIP Connectors MAJ2 ... MDJ2 Pin Assignment

J2/P2 Pin	Signal Name	Signal Name	J2/P2 Pin
1	Reserved [1])	Reserved [1])	2
3	Reserved [1])	Reserved [1])	4
5	+5V	+5V	6
7	+5V	+5V	8
9	REQ64# [2])	ACK64# [2])	10
11	+3.3V	+3.3V	12
13	AD00	AD01	14
15	AD02	GND	16
17	GND	AD03	18
19	AD04	AD05	20
21	AD06	+3.3V	22
23	+3.3V	AD07	24
25	C/BE0#	AD08	26
27	GND	GND	28
29	AD09	M66EN [3])	30
31	GND	AD10	32
33	AD11	AD12	34
35	AD13	GND	36
37	+3.3V	AD14	38
39	AD15	C/BE1#	40
41	PAR	+3.3V	42
43	GND	SERR#	44
45	SBO# [2])	+3.3V	46
47	SDONE [2])	PERR#	48
49	+3.3V	LOCK#	50
51	STOP#	GND	52
53	GND	DEVSEL#	54
55	TRDY#	+3.3V	56
57	GND	IRDY#	58
59	FRAME#	GND	60
61	+3.3V	C/BE2#	62
63	AD16	AD17	64
J2/P2 Pin	**Signal Name**	**Signal Name**	**J2/P2 Pin**

Notes:
[1]) These pin positions are reserved by the PC•MIP specification and not connected.
[2]) These pin positions are pulled to +3.3V via separate 4.7 KΩ resistors.
[3]) This pin positions is not connected on the CM1-COMBO.

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I/O Connectors MAJ3 ... MDJ3

The following table shows the pin assignment of the PC•MIP connectors MAJ3, MBJ3, MCJ3 and MDJ3 for the module slots A to D respectively.

PC•MIP Connectors MAJ3 ... MDJ3 Pin Assignment

J3/P3 Pin	Signal Name	Signal Name	J3/P3 Pin
1	I/O 01	I/O 02	2
3	I/O 03	I/O 04	4
5	GND	I/O 05	6
7	I/O 06	I/O 07	8
9	I/O 08	GND	10
11	I/O 09	I/O 10	12
13	GND	I/O 11	14
15	I/O 12	I/O 13	16
17	I/O 14	GND	18
19	I/O 15	I/O 16	20
21	GND	I/O 17	22
23	I/O 18	I/O 19	24
25	I/O 20	GND	26
27	I/O 21	I/O 22	28
29	GND	I/O 23	30
31	I/O 24	I/O 25	32
33	I/O 26	GND	34
35	I/O 27	I/O 28	36
37	GND	I/O 29	38
39	I/O 30	I/O 31	40
41	I/O 32	GND	42
43	I/O 33	I/O 34	44
45	GND	I/O 35	46
47	I/O 36	I/O 37	48
49	I/O 38	GND	50
51	I/O 39	I/O 40	52
53	GND	I/O 41	54
55	I/O 42	I/O 43	56
57	I/O 44	GND	58
59	I/O 45	I/O 46	60
61	I/O 47	I/O 48	62
63	I/O 49	I/O 50	64
J3/P3 Pin	**Signal Name**	**Signal Name**	**J3/P3 Pin**

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Mapping to *CompactPCI* ® I/O Connectors J4/P4 and J5/P5

The two next tables show the mapping of I/O signals from the PC•MIP modules to the *CompactPCI* ® connectors J4/P4 and J5/P5. The value in the column **I/O** specifies the module slot and number of the I/O signal feed to the corresponding pin. The column **MxJ3** gives the module slot and pin number of the PC•MIP modules J3 connector for that I/O signal. Example: On J4 pin A25 occurs the I/O signal 50 of PC•MIP module **C** which occurs also on **MCJ3** pin 64.

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Pin Mapping PC•MIP Module I/Os To *CompactPCI* Connector J4

#J4	A		B		C		D		E	
	I/O	MxJ3	I/O	MxJ3	I/O	MxJ3	I/O	MxJ3	I/O	MxJ3
25	C50	C64	C49	C63	C48	C62	C47	C61	C46	C60
24	C45	C59	C44	C57	C43	C56	C42	C55	C41	C54
23	C40	C52	C39	C51	C38	C49	C37	C48	C36	C47
22	C35	C46	C34	C44	C33	C43	C32	C41	C31	C40
21	C30	C39	C29	C38	C28	C36	C27	C35	C26	C33
20	C25	C32	C24	C31	C23	C30	C22	C28	C21	C27
19	C20	C25	C19	C24	C18	C23	C17	C22	C16	C20
18	C15	C19	C14	C17	C13	C16	C12	C15	C11	C14
17	C10	C12	C09	C11	C08	C09	C07	C08	C06	C07
16	C05	C06	C04	C04	C03	C03	C02	C02	C01	C01
15	+3.3V		+3.3V		+3.3V		+5V		+5V	
14										
13										
12										
11	D50	D64	D49	D63	D48	D62	D47	D61	D46	D60
10	D45	D59	D44	D57	D43	D56	D42	D55	D41	D54
9	D40	D52	D39	D51	D38	D49	D37	D48	D36	D47
8	D35	D46	D34	D44	D33	D43	D32	D41	D31	D40
7	D30	D39	D29	D38	D28	D36	D27	D35	D26	D33
6	D25	D32	D24	D31	D23	D30	D22	D28	D21	D27
5	D20	D25	D19	D24	D18	D23	D17	D22	D16	D20
4	D15	D19	D14	D17	D13	D16	D12	D15	D11	D14
3	D10	D12	D09	D11	D08	D09	D07	D08	D06	D07
2	D05	D06	D04	D04	D03	D03	D02	D02	D01	D01
1	+3.3V		+3.3V		+3.3V		+5V		+5V	
#J4	I/O	MxJ3	I/O	MxJ3	I/O	MxJ3	I/O	MxJ3	I/O	MxJ3
	A		B		C		D		E	

Pin Mapping PC•MIP Module I/Os To *CompactPCI* Connector J5

#J5	A		B		C		D		E	
	I/O	**MxJ3**	**I/O**	**MxJ3**	**I/O**	**MxJ3**	**I/O**	**MxJ3**	**I/O**	**MxJ3**
22	A50	A64	A49	A63	A48	A62	A47	A61	A46	A60
21	A45	A59	A44	A57	A43	A56	A42	A55	A41	A54
20	A40	A52	A39	A51	A38	A49	A37	A48	A36	A47
19	A35	A46	A34	A44	A33	A43	A32	A41	A31	A40
18	A30	A39	A29	A38	A28	A36	A27	A35	A26	A33
17	A25	A32	A24	A31	A23	A30	A22	A28	A21	A27
16	A20	A25	A19	A24	A18	A23	A17	A22	A16	A20
15	A15	A19	A14	A17	A13	A16	A12	A15	A11	A14
14	A10	A12	A09	A11	A08	A09	A07	A08	A06	A07
13	A05	A06	A04	A04	A03	A03	A02	A02	A01	A01
12	+3.3V		+3.3V		+3.3V		+5V		+5V	
11	B50	B64	B49	B63	B48	B62	B47	B61	B46	B60
10	B45	B59	B44	B57	B43	B56	B42	B55	B41	B54
9	B40	B52	B39	B51	B38	B49	B37	B48	B36	B47
8	B35	B46	B34	B44	B33	B43	B32	B41	B31	B40
7	B30	B39	B29	B38	B28	B36	B27	B35	B26	B33
6	B25	B32	B24	B31	B23	B30	B22	B28	B21	B27
5	B20	B25	B19	B24	B18	B23	B17	B22	B16	B20
4	B15	B19	B14	B17	B13	B16	B12	B15	B11	B14
3	B10	B12	B09	B11	B08	B09	B07	B08	B06	B07
2	B05	B06	B04	B04	B03	B03	B02	B02	B01	B01
1	+3.3V		+3.3V		+3.3V		+5V		+5V	
#J5	**I/O**	**MxJ3**	**I/O**	**MxJ3**	**I/O**	**MxJ3**	**I/O**	**MxJ3**	**I/O**	**MxJ3**
	A		**B**		**C**		**D**		**E**	

Technical Specifications

System-Processor i960®RP and local Devices

- CPU Core
  - Based on the i960JF high performance core
  - Highest throughput at low power consumption (33 MHz/3.3 V)
  - Integrated 4 KB instruction and 2 KB data cache
  - 1 KB internal data RAM

- Memory
  - 8 MB FPM or EDO DRAM
  - 4 MB Flash ROM (32-Bit), on-board programmable
  - Up to 4 KB burst transfers
  - 32 Kbit serial EEPROM

- I/O
  - RS232 serial interface, D-SUB9 front panel connector, 50-115 kBit/s
  - ACCESS.bus-interface (SMBus, I^2C) across 4-pole pin header

- PCI-to-PCI Bridge
  - Dual 64 Byte posting buffer for data transfer rate acceleration
  - Forwards memory, I/O, configuration commands from PCI bus to PCI bus
  - local devices and memory accessible from *CompactPCI* ® bus including Flash ROM programming
  - Conforms to *PCI-to-PCI Bridge Architecture Specification*, revision 1.0

- Diagnostics/Debugging
  - Red LED: i960RP initializing fault
  - Yellow LED: access to PC•MIP module(s)
  - Green LED: access to local peripherals or memory
  - Reset push button switch (optional)
  - NMI push button switch (optional)

CompactPCI ® Bus

- 6 U height, 20.32 mm width
- 32-Bit PCI interface 33 MHz (max. data transfer rate 132 MB/s)
- PCI 64-Bit dual address cycles
- Up to 64 byte PCI bursts
- $V_{I/O}$=5V
- Complies to *CompactPCI* ® *Specification*, revision 2.1

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PC•MIP Slots

- PC•MIP Bus Interface
  - 32-Bit PCI interface, 33 MHz, $V_{I/O}$=3.3V
- Module Types
  - 4 PC•MIP landing zones (A-D) for type I or type II modules (I/O across *CompactPCI* ® J4/J5 or module front connector)
  - Neighboring slots (A-B, C-D) can carry double-size modules
- Connectors
  - 3 each 64-pole free height connector according IEEE 1386 for any PC•MIP slot
- Complies to *PC•MIP Draft Specification 0.93* (ANSI/VITA Task Group VITA-29)

Power Consumption

- +5 V ± 5% 600 mA max., without PC•MIP module(s)
- +3.3 V ± 0.3V 1.1 A max., without PC•MIP module(s)
- +12 V ± 5% 0 mA max., without PC•MIP module(s)
- -12 V ±5 % 0 mA max., without PC•MIP module(s)

Temperature, Humidity

- Operating temperature 0-70˚ C
- Humidity 5-90%, non condensing

Technical specifications are subject to change

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Ordering Information

Ordering Information

Short Alias	Ordering No.	Description
COMBO	CM1-1-COMBO	6U intelligent Carrier for 4 PC•MIP Modules, CPU i960RP 33MHz, 8MB DRAM, 4MB Flash ROM, RS232 Serial Port, *CompactPCI* Interface 32-Bit
USB	CMA-1-USB	PCMIP Type II single size module 10H, USB 1.1 12Mbps OHCI controller
1394	CMF-1-1394	PCMIP Type II single size module 10H, IEEE 1394 OHCI FireWire Controller, 400Mbps
ISDN	CMI-1-ISDN	PCMIP Type II single size module 10H, ISDN S/T (S0) terminal adapter
ETH	CMN-1-ETH	PCMIP Type II single size module 10H, 10/100Mbps Ethernet Controller RJ45

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